CLAIMS AMENDMENTS:

Claim 1 (Original): An adder having as inputs a first and a second data inputs, a first and a second carry inputs, and a carry selection input, comprising:

a first XOR element for generating an XOR output of the first and the second data inputs;

a first multiplexer for selecting one of the first carry input or the first data input while the XOR output is made a selection signal;

a second multiplexer for selecting one of the second carry input or the second data input;

a third multiplexer for selecting one of the first or the second carry inputs while the carry selection input is made a selection signal; and

a second XOR element for generating an XOR output of an output of the third multiplexer and the XOR output, wherein

an output of the first multiplexer is made a first carry output,

an output of the second multiplexer is made a second carry output, and

an output of the third multiplexer is made an addition value.

Claim 2 (Original): An adder comprising plural adders each of which is recited in claim 1 and which are continuously connected to each other, wherein:

a first carry output of a preceding stage is made a carry input of a subsequent stage;

a second carry output of the preceding stage is made a second carry input of the subsequent stage;

a carry selection input of the plural adders is made common to all stages;

a true carry input of an initial stage adder is made the carry selection input, the first carry input is made a first virtual carry, and the second carry input is made a second virtual carry;

the adder further comprises a fourth multiplexer for selecting one of a first or a second carry outputs of a final stage adder by the carry selection input; and

an output of the fourth multiplexer is made a carry output.

Claim 3 (Original): An adder according to claim 2, wherein the third multiplexer of the initial stage adder is omitted, and instead of an output of the third multiplexer of the initial stage adder, the carry selection input is used.

Claim 4 (Currently Amended): An adder comprising plural adders each of which is recited in claim 2 ~~or 3~~ and which are continuously connected to each other, wherein

a carry output of a preceding stage is made a carry input of a subsequent stage, and

except for a final stage adder, the number of bits which can be processed by an adder of each stage is equal to or larger than the number of bits which can be processed by an adder of a preceding stage.

Claim 5 (Original): An adder according to claim 4, wherein except for an initial stage adder, a difference between the number of bits which can be processed by the adder of each stage and the number of bits which can be processed by the adder of the preceding stage is made constant.

Claim 6 (Original): A booth multiplier configured by a tree structure, wherein an adder of claim 4 is used as a final stage adder.

Claim 7 (New): An adder comprising plural adders each of which is recited in claim 3 and which are continuously connected to each other, wherein

a carry output of a preceding stage is made a carry input of a subsequent stage, and

except for a final stage adder, the number of bits which can be processed by an adder of each stage is equal to or larger than the number of bits which can be processed by an adder of a preceding stage.

Claim 8 (New): An adder according to claim 7, wherein except for an initial stage adder, a difference between the number of bits which can be processed by the adder of each stage and the number of bits which can be processed by the adder of the preceding stage is made constant.

Claim 9 (New): A booth multiplier configured by a tree structure, wherein an adder of claim 7 is used as a final stage adder.